

# EXHIBIT 1

# ARM® CoreTile Express A15×2 A7×3

Cortex®-A15\_A7 MPCore (V2P-CA15\_A7)

## Technical Reference Manual



## ARM CoreTile Express A15×2 A7×3 Technical Reference Manual

Copyright © 2012-2014, 2016 ARM Limited or its affiliates. All rights reserved.

### Release Information

The following changes have been made to this book.

Change history			
Date	Issue	Confidentiality	Change
June 2012	A	Non-Confidential	First release for V2P-CA15_A7
July 2012	B	Non-Confidential	Second release for V2P-CA15_A7
10 August 2012	C	Non-Confidential	Third release for V2P-CA15_A7
12 October 2012	D	Non-Confidential	Fourth release for V2P-CA15_A7
31 March 2013	E	Non-Confidential	Fifth release for V2P-CA15_A7
28 June 2013	F	Non-Confidential	Sixth release for V2P-CA15_A7
16 October 2013	G	Non-Confidential	Seventh release for V2P-CA15_A7
29 May 2014	H	Non-Confidential	Eighth release for V2P-CA15_A7
16 December 2016	I	Non-Confidential	Ninth release for V2P-CA15_A7

### Proprietary Notice

This document is protected by copyright and other related rights and the practice or implementation of the information contained in this document may be protected by one or more patents or pending patent applications. No part of this document may be reproduced in any form by any means without the express prior written permission of ARM. **No license, express or implied, by estoppel or otherwise to any intellectual property rights is granted by this document unless specifically stated.**

Your access to the information in this document is conditional upon your acceptance that you will not use or permit others to use the information for the purposes of determining whether implementations infringe any third party patents.

THIS DOCUMENT IS PROVIDED “AS IS”. ARM PROVIDES NO REPRESENTATIONS AND NO WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY, SATISFACTORY QUALITY, NON-INFRINGEMENT OR FITNESS FOR A PARTICULAR PURPOSE WITH RESPECT TO THE DOCUMENT. For the avoidance of doubt, ARM makes no representation with respect to, and has undertaken no analysis to identify or understand the scope and content of, third party patents, copyrights, trade secrets, or other rights.

This document may include technical inaccuracies or typographical errors.

TO THE EXTENT NOT PROHIBITED BY LAW, IN NO EVENT WILL ARM BE LIABLE FOR ANY DAMAGES, INCLUDING WITHOUT LIMITATION ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES, HOWEVER CAUSED AND REGARDLESS OF THE THEORY OF LIABILITY, ARISING OUT OF ANY USE OF THIS DOCUMENT, EVEN IF ARM HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

This document consists solely of commercial items. You shall be responsible for ensuring that any use, duplication or disclosure of this document complies fully with any relevant export laws and regulations to assure that this document or any portion thereof is not exported, directly or indirectly, in violation of such export laws. Use of the word “partner” in reference to ARM’s customers is not intended to create or refer to any partnership relationship with any other company. ARM may make changes to this document at any time and without notice.

If any of the provisions contained in these terms conflict with any of the provisions of any signed written agreement covering this document with ARM, then the signed written agreement prevails over and supersedes the conflicting provisions of these terms.

Words and logos marked with ® or ™ are registered trademarks or trademarks of ARM Limited or its affiliates in the EU and/or elsewhere. All rights reserved. Other brands and names mentioned in this document may be the trademarks of their respective owners. Please follow ARM's trademark usage guidelines at , <http://www.arm.com/about/trademarks/guidelines/index.php>

Copyright © 2012-2014, 2016 ARM Limited or its affiliates. All rights reserved.

ARM Limited. Company 02557590 registered in England.

110 Fulbourn Road, Cambridge, England CB1 9NJ.

LES-PRE-20349

#### **Confidentiality Status**

This document is Non-Confidential. The right to use, copy and disclose this document may be subject to license restrictions in accordance with the terms of the agreement entered into by ARM and the party that ARM delivered this document to.

#### **Product Status**

The information in this document is final, that is for a developed product.

#### **Web Address**

<http://www.arm.com>

# Contents

## ARM CoreTile Express A15×2 A7×3 Technical Reference Manual

	<b>Preface</b>	
	About this book .....	viii
	Feedback .....	xii
<b>Chapter 1</b>	<b>Introduction</b>	
	1.1 About the CoreTile Express A15×2 A7×3 daughterboard .....	1-2
	1.2 Precautions .....	1-4
<b>Chapter 2</b>	<b>Hardware Description</b>	
	2.1 CoreTile Express A15×2 A7×3 daughterboard architecture .....	2-2
	2.2 Cortex-A15_A7 MPCore test chip .....	2-4
	2.3 System interconnect signals .....	2-6
	2.4 Power-up configuration and resets .....	2-10
	2.5 Serial Configuration Controller (SCC) .....	2-21
	2.6 Voltage control and process monitors .....	2-22
	2.7 Clocks .....	2-24
	2.8 Interrupts .....	2-34
	2.9 HDLCD .....	2-38
	2.10 DDR2 memory interface .....	2-39
	2.11 Debug .....	2-40
<b>Chapter 3</b>	<b>Programmers Model</b>	
	3.1 About this programmers model .....	3-2
	3.2 Daughterboard memory map .....	3-3
	3.3 Test chip SCC registers .....	3-12
	3.4 Programmable peripherals and interfaces .....	3-54

<b>Appendix A</b>	<b>Signal Descriptions</b>	
	A.1 Daughterboard connectors .....	A-2
	A.2 HDRX HSB multiplexing scheme .....	A-3
	A.3 Header connectors .....	A-5
	A.4 Debug and trace connectors .....	A-6
<b>Appendix B</b>	<b>HDLCD controller</b>	
	B.1 Introduction .....	B-2
	B.2 HDLCD Programmers Model .....	B-3
<b>Appendix C</b>	<b>Electrical Specifications</b>	
	C.1 AC characteristics .....	C-2
<b>Appendix D</b>	<b>Revisions</b>	

## About this book

This book is for the CoreTile Express A15×2 A7×3 daughterboard.

## Intended audience

This document is written for experienced hardware and software developers to aid the development of ARM-based products using the CoreTile Express A15×2 A7×3 daughterboard with the Motherboard Express µATX as part of a development system.

## Using this book

This book is organized into the following chapters:

### Chapter 1 *Introduction*

Read this for an introduction to the CoreTile Express A15×2 A7×3 daughterboard.

### Chapter 2 *Hardware Description*

Read this for a description of the hardware present on the daughterboard.

### Chapter 3 *Programmers Model*

Read this for a description of the configuration registers present on the daughterboard.

### Appendix A *Signal Descriptions*

Read this for a description of the signals present on the daughterboard.

### Appendix B *HDLCD controller*

Read this for a description of the HDLCD controller in the Cortex-A15\_A7 test chip.

### Appendix C *Electrical Specifications*

Read this for a description of the electrical specifications of the daughterboard.

### Appendix D *Revisions*

Read this for a description of the technical changes between released issues of this book.

## Glossary

The *ARM Glossary* is a list of terms used in ARM documentation, together with definitions for those terms. The *ARM Glossary* does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See *ARM Glossary*, <http://infocenter.arm.com/help/topic/com.arm.doc.aeg0014-/index.html>.

## Conventions

This book uses the conventions that are described in:

- *Typographical conventions* on page ix
- *Timing diagrams* on page ix
- *Signals* on page x.

# Chapter 1

## Introduction

This chapter provides an introduction to the CoreTile Express A15×2 A7×3 daughterboard. It contains the following sections:

- *About the CoreTile Express A15×2 A7×3 daughterboard* on page 1-2
- *Precautions* on page 1-4.



## 1.1 About the CoreTile Express A15×2 A7×3 daughterboard

The CoreTile Express A15×2 A7×3 daughterboard is designed as a platform for developing systems based on *Advanced Microcontroller Bus Architecture* (AMBA) that use the *Advanced eXtensible Interface* (AXI) or custom logic for use with ARM cores.

You can use the CoreTile Express A15×2 A7×3 daughterboard to create prototype systems.

---

### Note

---

You can use the CoreTile Express A15×2 A7×3 daughterboard with a Motherboard Express µATX. See [System interconnect signals on page 2-6](#) for information about interconnection.

You can also use the CoreTile Express daughterboard with a custom-design motherboard. See *ARM® Programmer Module (V2M-CP1)*.

---

The daughterboard includes the following features:

- Cortex-A15\_A7 MPCore test chip, with NEON™, that is, the advanced *Single Instruction Multiple Data* (SIMD) extension, and *Floating Point Unit* (FPU), that contains a dual-core A15 cluster operating at 1GHz and a triple-core A7 cluster operating at 800MHz.
- Cortex-A15\_A7 MPCore test chip internal AXI subsystem operating at 500MHz.
- Simple configuration with V2M-P1 motherboard:
  - Configuration EEPROM.
  - Daughterboard Configuration Controller.
- Nine programmable oscillators.
- 2GB of daughterboard DDR2 32-bit memory operating at 400MHz.
- *High Definition LCD* (HDLCD) controller that supports up to 1920×1080p video at 60Hz, 165MHz pixel clock.
- CoreSight software debug and 32-bit trace ports.
- HDRX header with one multiplexed AMBA AXI master bus port that connects to the other daughterboard site on the V2M-P1 motherboard.
- HDRY header with four buses to the motherboard:
  - *Static Memory Bus* (SMB).
  - *MultiMedia Bus* (MMB).
  - *Configuration Bus* (CB).
  - *System Bus* (SB).
- *Power Supply Units* (PSUs) for the Cortex-A15\_A7 test chip and DDR2 memory.
- Core voltage control and current, temperature, and power monitoring.
- On-board energy meter.

---

### Note

---

The Cortex-A15\_A7 test chip does not support TrustZone®.

---

[Figure 1-1 on page 1-3](#) shows the layout of the daughterboard:

## 2.2 Cortex-A15\_A7 MPCore test chip

Figure 2-2 shows the main components of the test chip.

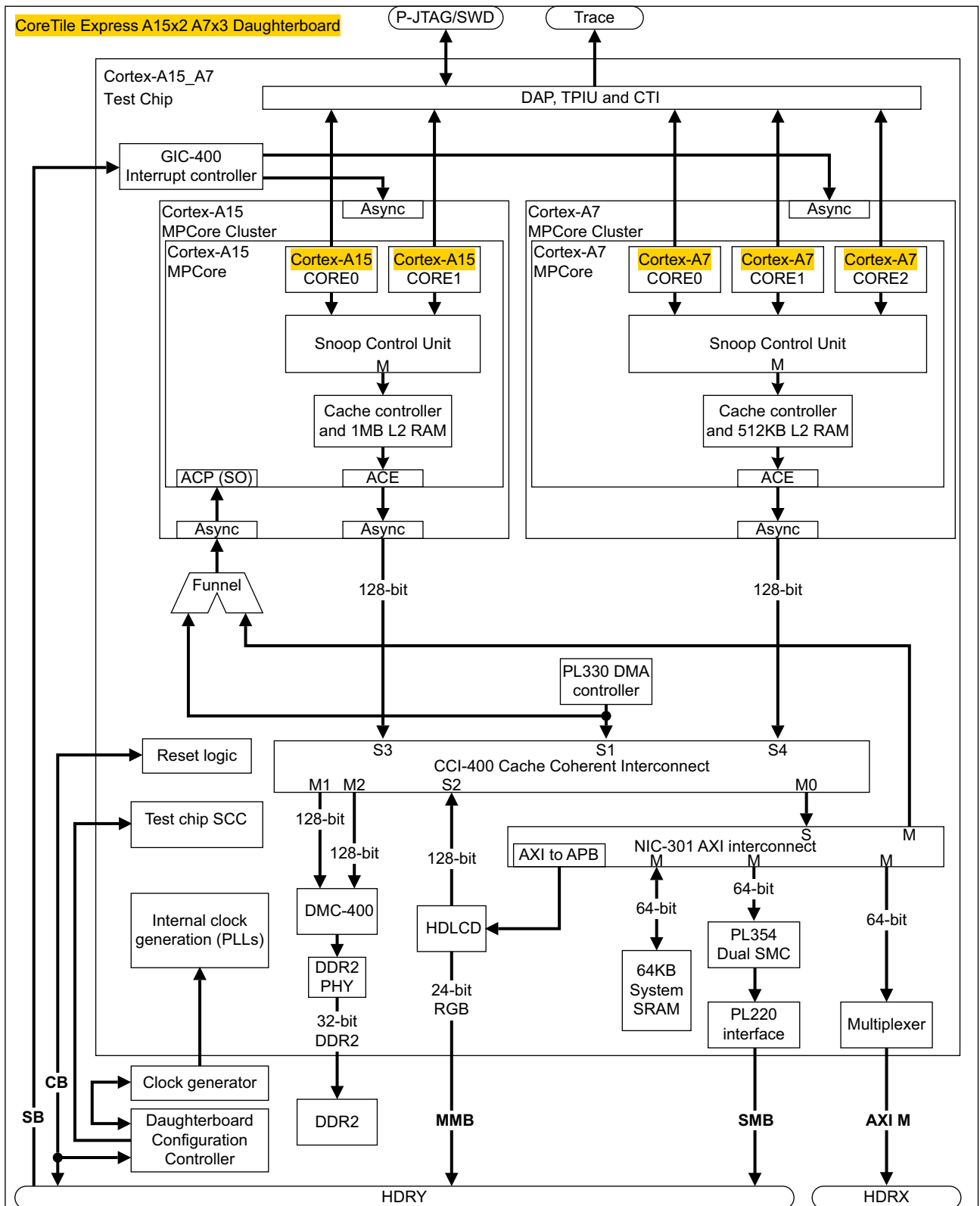


Figure 2-2 Top-level view of the Cortex-A15\_A7 MPCore test chip components

---

**Note**

---

Bus lines with single-headed arrows indicate the direction of control, not the direction of data flow. That is, each arrow points from bus master to bus slave.

---

**Cortex-A15\_A7 MPCore test chip**

The test chip includes the following components and interfaces:

- **Cortex-A15 dual-core** cluster operating at 1GHz:
  - Version r2p1.
  - 32KB I/D cache.
  - NEON and *Floating Point Unit* (FPU).
  - ACP port.
  - 1MB L2 cache.
  - *Dual Program Flow Trace Macrocell* (PTM).
- **Cortex-A7 triple-core** cluster operating at 800MHz:
  - Version r0p1.
  - 32KB I/D cache.
  - NEON and FPU.
  - 512KB L2 cache.
  - *Dual Embedded Trace Macrocell* (ETM).
- NIC-301 AXI interconnect operating at 500MHz.
- CCI-400 cache coherent interconnect operating at 500MHz that provides cache-coherency between the two clusters.
- DMC-400 32-bit *Double Data Rate 2* (DDR2) *Dynamic Memory Controller* (DMC) interface to the onboard 2GB DDR2 memory.
- PL354 32-bit SMB controller (SMC). This connects to the motherboard peripherals.
- PL330 *Direct Memory Access* (DMA) controller.
- 24-bit HDLCD video controller that drives the MMB to the MUXFPGA on the V2M-P1 Motherboard Express.
- Multiplexed 64-bit AXI master interface.
- 64KB of local on-chip SRAM.
- CoreSight debug and trace interface to the onboard connectors:
  - PTM for each Cortex-A15 core.
  - ETM for each Cortex-A7 core.
  - 16KB ETB.
  - DAP.
  - *Trace Port Interface Unit* (TPIU) for real-time trace data.
  - JTAG interface for debug.
- *Serial Configuration Controller* (SCC) interface:
  - Interfaces to the Daughterboard Configuration Controller.
  - Configures the test chip *Phase-Locked Loops* (PLLs) during power up or reset.
- Interrupts interface:
  - Connects interrupt signals from the V2M-P1 motherboard to the *Generic Interrupt Controller* (GIC) in the test chip.

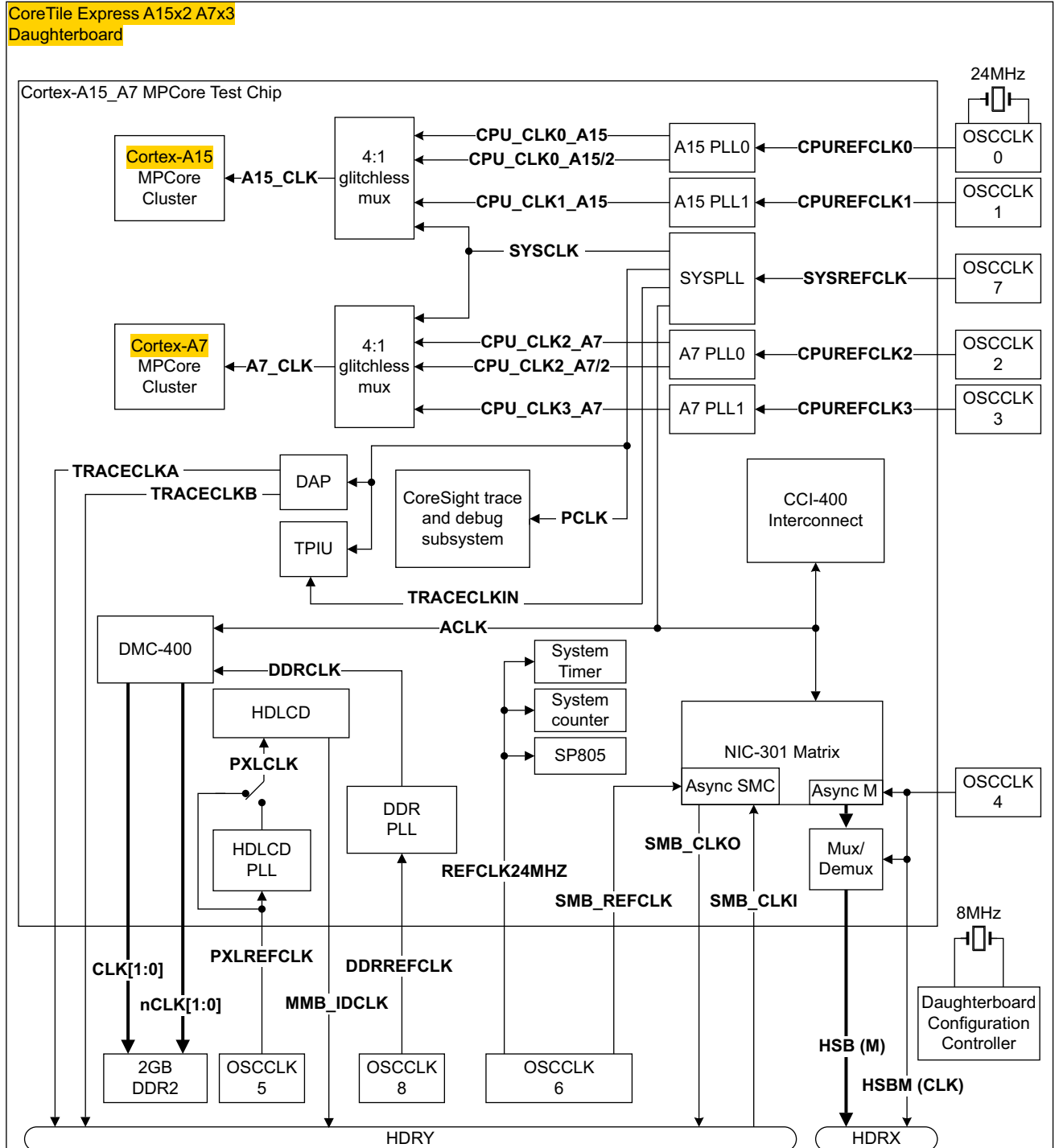


Figure 2-10 CoreTile Express A15x2 A7x3 daughterboard clocks

Figure 2-10 shows the default inputs for the PLLs. You can independently select **SYSREFCLK** as the inputs to any or all of:

- A15 PLL0.
- A15 PLL1.
- A7 PLL0.
- A7 PLL1.
- HDLCD PLL.

- DDR PLL.

See [Test chip SCC Register 11 on page 3-27](#).

CPU\_CLK0\_A15 is the default source for A15\_CLK.

CPU\_CLK2\_A7 is the default source for A7\_CLK.

You can use the 4-way glitchless multiplexers to select any of the four inputs as the sources for A15\_CLK and A7\_CLK. See [Test chip SCC Register 11 on page 3-27](#).

When you write to the SCC registers to change the sources for the MPCore clocks, you can monitor when the change takes effect by reading the clock status register. See [Test chip SCC Register 12 on page 3-30](#).

You can select the polarity of MMB\_IDCLK relative to PXLREFCLK. It can be either in phase with PXLREFCLK or inverted. See [Polarities Register bit assignments on page B-17](#).

You can also use the SCC registers to exercise other options, for example, to select *External Bypass* to bypass the PLL and drive the reference clock into the design.

#### ———— Note ————

The configuration process bypasses the HDLCD PLL by default.

ARM does not recommend that you select non-default options for the other PLLs and [Figure 2-10 on page 2-26](#) does not show these options. See [Test chip SCC Register 11 on page 3-27](#) and [Test chip SCC Registers 13, 15, 17, 19, 23, and 25 PLL control registers on page 3-31](#).

The MCC and Daughterboard Configuration Controller use the board.txt configuration file for the daughterboard to set the frequency of the daughterboard clock generators and to configure the SCC registers on power-up or reset. You can also adjust the daughterboard clocks during run-time by using the motherboard SYS\_CFG register interface.

For more information see:

- [Power-up configuration and resets on page 2-10](#).
- *Versatile™ Express Configuration Technical Reference Manual* for an example board.txt file.
- *Motherboard Express μATX Technical Reference Manual*.

## 2.7.2 Daughterboard programmable clock generators

This section describes the daughterboard clock generators and the clocks that the test chip generates from them to drive the on-chip systems.

The following SCC registers control the PLLs, clock divider blocks and PLL input select multiplexers:

- [Test chip SCC Register 11 on page 3-27](#)
- [Test chip SCC Register 12 on page 3-30](#)
- [Test chip SCC Registers 13, 15, 17, 19, 23, and 25 PLL control registers on page 3-31](#)
- [Test chip SCC Registers 14, 16, 18, 22, 24 and 26 PLL value registers on page 3-33](#).